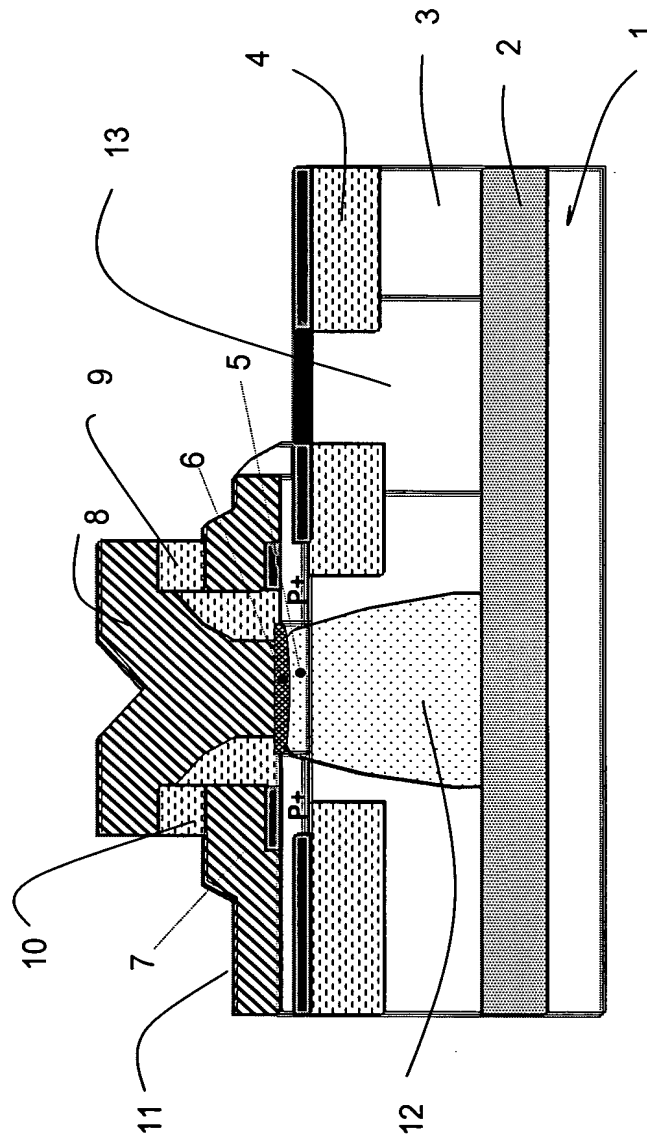


FIG. 1 (Prior Art)



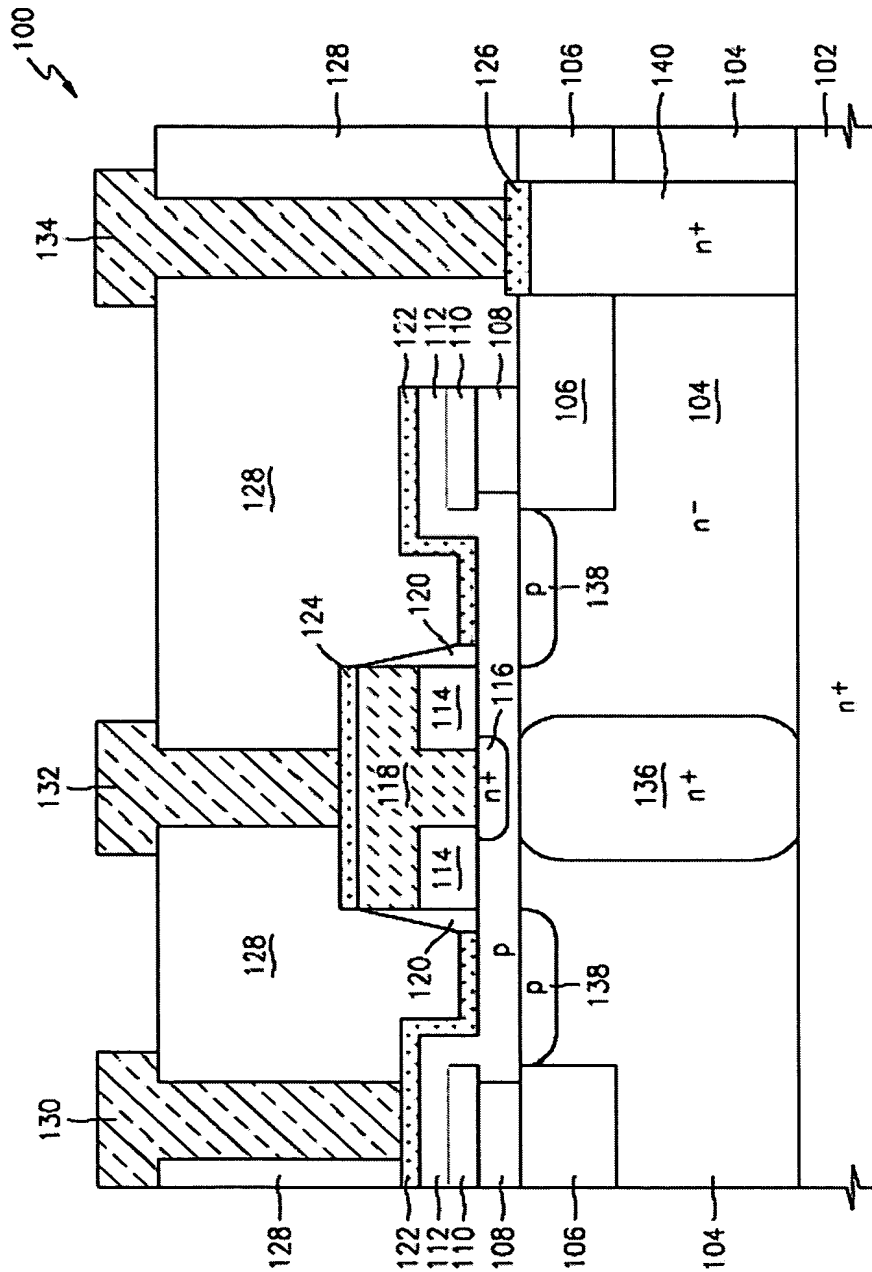


FIG. 2

FIG. 3(A)

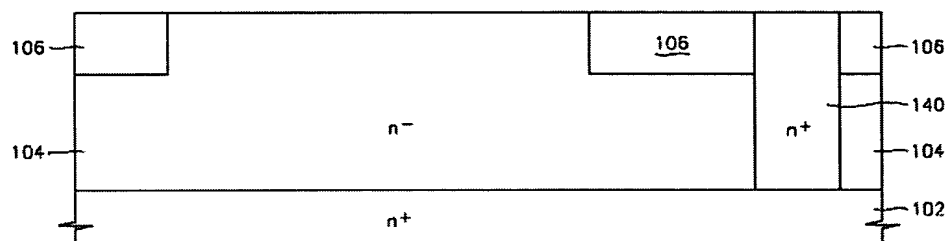


FIG. 3(B)

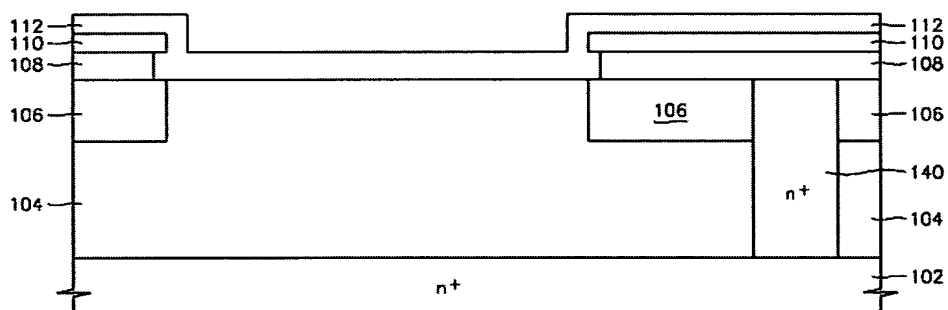


FIG. 3(C)

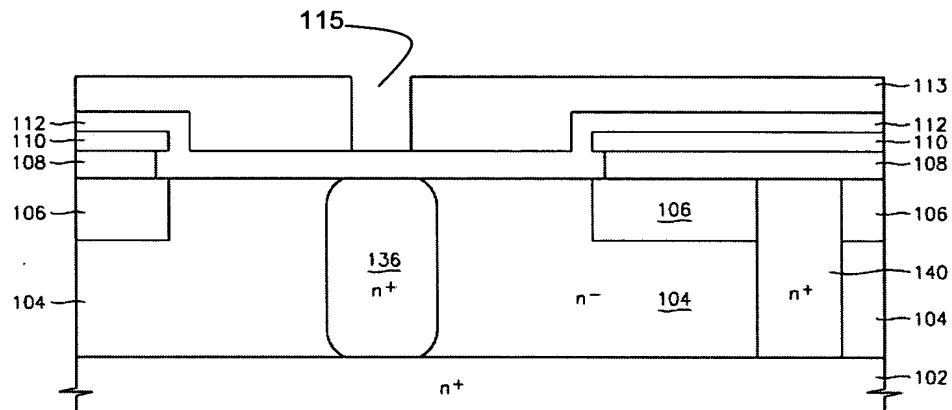
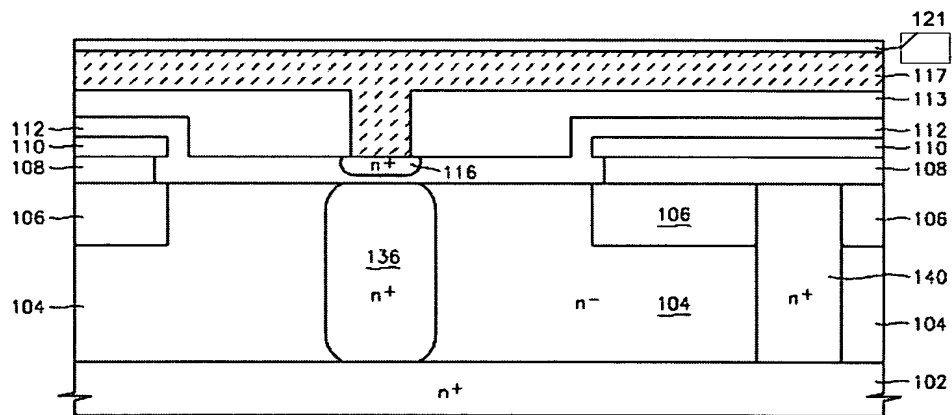


FIG. 3(D)



A cross-sectional view of a semiconductor device. The structure is built on a substrate labeled n^+ at the bottom. A central region is labeled 136 and n^+ . To the left and right of this central region are regions labeled 138 and P . Above these P regions are regions labeled 106 and 104 . The rightmost region is labeled n^+ . The top surface is covered by a layer labeled 110 , with a thin layer labeled 112 on top. A central contact region is labeled 116 and n^+ . Above this contact region is a structure labeled 118 with a hatched pattern. The structure 118 is flanked by regions labeled 120 and 114 . The leftmost region is labeled 104 and 106 .

This cross-sectional view shows a semiconductor device with a central gate stack and side gates. The central gate stack includes a gate dielectric layer 118, a gate electrode 114, and a gate contact 124. The side gates include a gate dielectric layer 120, a gate electrode 114, and a gate contact 126. The device is formed on a substrate 102 with an n⁺ layer. The channel region is n⁻ 104. The source and drain regions are p⁺ 106. The gate stack is formed on a p⁺ 116 layer. The side gates are formed on n⁺ 140 regions. The device is surrounded by a passivation layer 128. The top surface is covered by a passivation layer 141 and 143. The bottom surface is covered by a passivation layer 102.

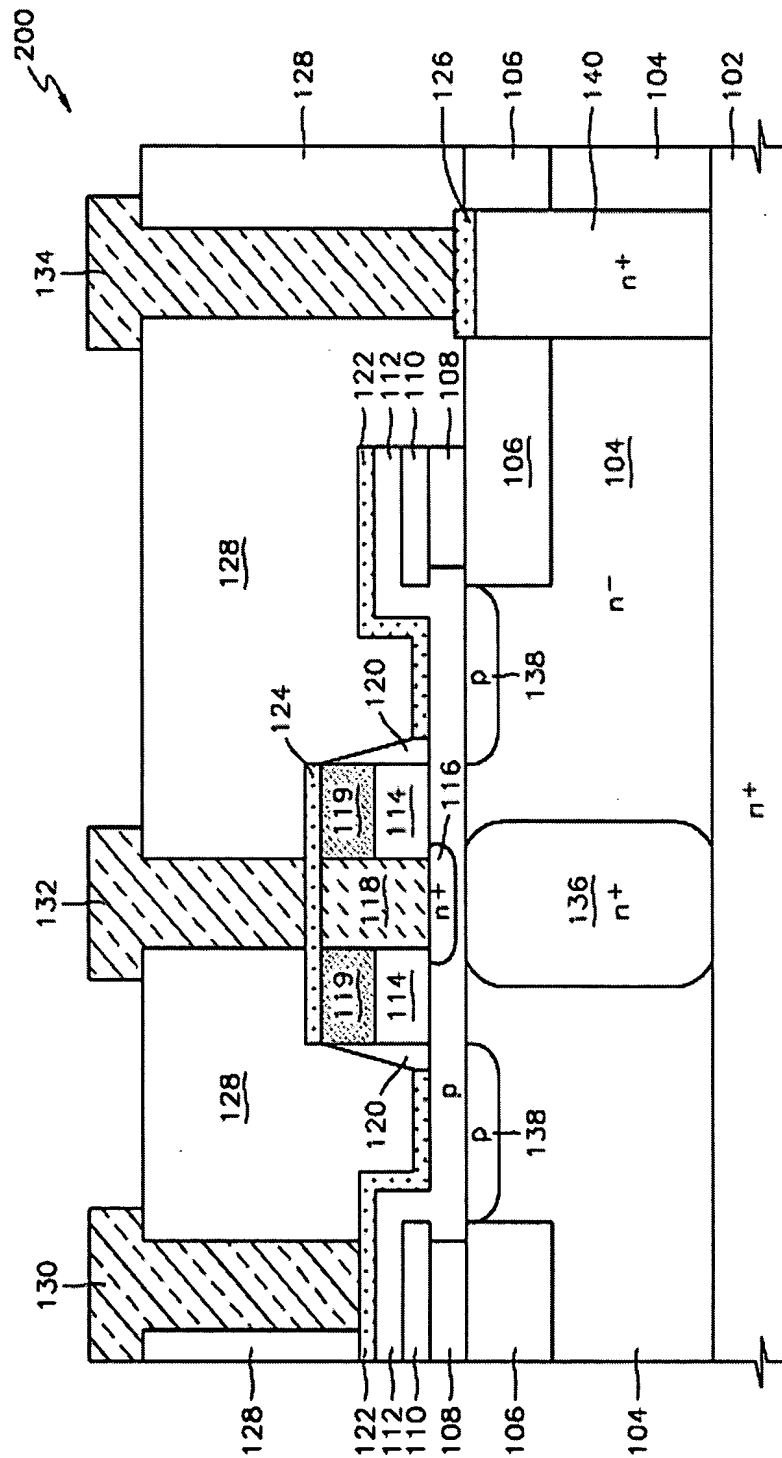


FIG. 4

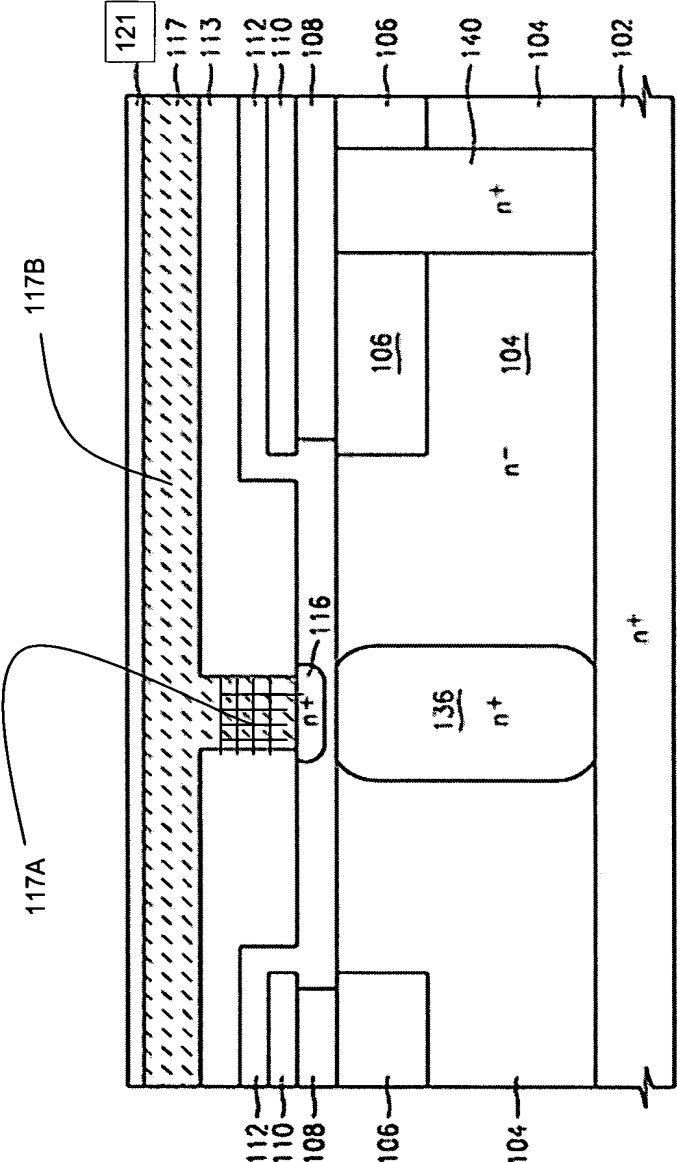


FIG. 5

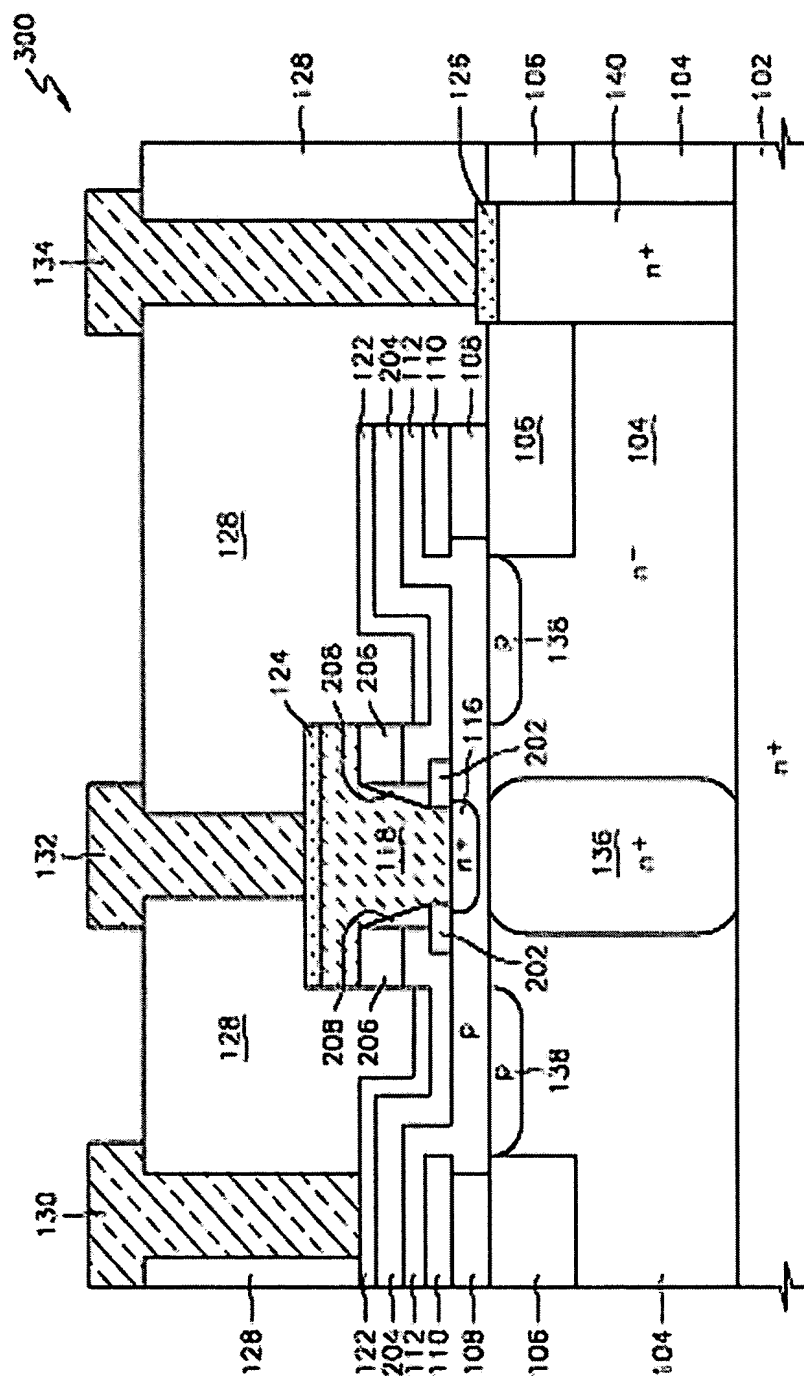


FIG. 6

FIG. 7(A)

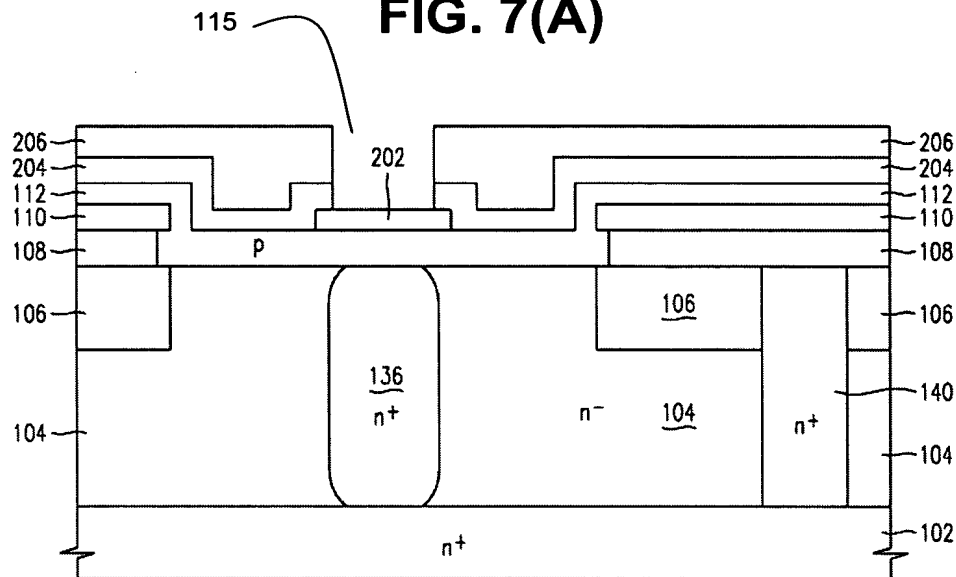


FIG. 7(B)

